Section III. REMARKS

Affirmation of Prior Election and Withdrawal of Claim 62

Applicants acknowledge, with traverse, the Examiner's finalization of the restriction requirement imposed against claims 39-76 in the June 2, 2003 Office Action. Claims 39-60, 68-69 and 72-76 have been withdrawn herein.

In the September 15, 2003 Office Action, the Examiner imposed an additional restriction requirement against claims 61-67 and 70-71 and required that an election be made between:

Group I:	Claims 61, 63-67 and 70-71, drawn to a method, classified in class 117, subclass 84; and
Group II:	Claim 62, drawn to a product, classified in class 257, subclass 615.

Applicants hereby affirm the prior provisional election made by Steven J. Hultquist during a telephone conversation with Examiner Song on August 27, 2003, **electing the Group I claims**.

Consistent with such prior election and present affirmation, the non-elected Group II claim 62 has been withdrawn herein.

The pending claims in the application therefore are claims 61, 63-67 and 70-71.

Priority

In response to the remarks at page 3 of the September 15, 2003 Office Action, concerning the priority claim, the specification has been amended on the title page thereof, under the heading "Cross Reference to Related Applications," to specify the present application as a continuation of U.S. Patent Application No. 08/955,168 filed October 21, 1997, to which priority is claimed.

Double Patenting Rejection, and Submission of Terminal Disclaimer Obviating Same

In the September 15, 2003 Office Action, claims 61, 63-67 and 70-71 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-18 of Tischler et al. U.S. Patent No. 5,679,152.

In response, a Terminal Disclaimer is enclosed and submitted herewith under the provisions of 37 C.F.R. §1.321(c), to overcome the obviousness-type double patenting rejection.

Rejection of Claims Under §§102/103, and Traversal Thereof

In the September 15, 2003 Office Action:

claims 61 and 63-67 were rejected under 35 U.S.C. §102(e) as anticipated by Akasaki et al. (U.S. Patent No. 5,846,844); and

claims 70-71 were rejected under 35 U.S.C. §103(a) as unpatentable over Gmitter et al. (U.S. Patent No. 4,883,561) in view of Akasaki et al.

These rejections are traversed and reconsideration of the patentability of the pending claims 61, 63-67 and 70-71 is requested, in light of the following remarks.

Rejection under 35 U.S.C. §102(e)

In the September 15, 2003 Office Action, claims 61 and 63-67 were rejected under 35 U.S.C. §102(e) as anticipated by Akasaki et al. (U.S. Patent No. 5,846,844) (hereinafter Akasaki).

Such rejection of claims is traversed, on the basis of the enclosed Declaration under 37 C.F.R. §1.131 of inventor Michael A. Tischler, attesting to facts showing conception prior to the effective date of Akasaki coupled with due diligence from prior to the effective date of Akasaki to the filing date of the grandparent of the instant application, from which the present application claims priority.

As set out in the Michael A. Tischler Declaration, Akasaki's priority date is November 29, 1993. The Michael A. Tischler Declaration attests to facts showing conception of the instant claimed invention prior to the November 29, 1993 Akasaki priority date coupled with due diligence from prior to November 29, 1993 to the filing date of the grandparent application of the instant application, January 27, 1994.

The Michael A. Tischler Declaration thereby removes Akasaki as competent prior art.

The Akasaki reference is not competent prior art. The §102(e) rejection is obviated by the Tischler Declaration.

Withdrawal of the rejection of claims 61 and 63-67 therefore is respectfully requested.

Rejection under 35 U.S.C. §103(a)

In the September 15, 2003 Office Action, claims 70-71 were rejected under 35 U.S.C. §103(a) as being unpatentable over Gmitter et al. (U.S. Patent No. 4,883,561) (hereinafter Gmitter '561) in view of Akasaki. Applicants traverse such rejection.

Since Akasaki has been removed as competent prior art, the rejection of claims 70-71 relies solely on Gmitter '561.

Gmitter '561 is directed to a process for selectively lifting off an epitaxial film from a single crystal substrate on which it has been grown. For ease of reference, Figure 2 of Gmitter '561 is reproduced below. Gmitter '561 describes deposition of epitaxial GaAs layer(s) **3**, **4** onto a thin release layer **2** previously deposited on substrate **1**. A detachable polymeric support layer **25** then is applied, under tension, over GaAs epitaxial layer(s) **3**, **4**. Next, the thin release layer **2** is selectively etched away by acid, causing the released edges of the GaAs epitaxial film layer(s) **3**, **4** to curl upward due to tension of the polymeric support layer **25**, as illustrated in Figure 2. Eventually, the composite layer structure, including the GaAs epitaxial film layer(s) **3**, **4** and the polymeric support layer **25** attached thereto, is lifted away from the substrate **1**.

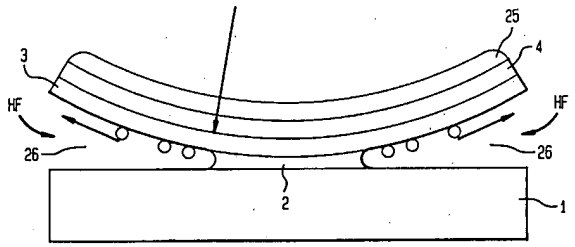


FIG. 2 of Gmitter '561

Gmitter `561 fails to teach or suggest applicants' claimed invention.

Applicants' claim 70 recites:

> **"70. A method of forming a GaN single crystal substrate, comprising:**
>
> **growing GaN on a gallium arsenide substrate; and**
>
> **etching the gallium arsenide substrate to remove same and yield the GaN single crystal substrate."**

Gmitter '561 **teaches away** from such methodology. At column 1, lines 11-15, Gmitter '561 discloses that:

> **"[T]his invention [of Gmitter et al.] relates to epitaxially grown films and devices and more particularly to a method of releasing such films and/or devices from the single crystal substrate upon which it is formed to enable its transfer to other substrates and reuse of the single crystal substrate." (Gmitter '561, column 1, lines 11-15)**

Thus, **opposite to applicants' claimed invention**, the base substrate of Gmitter '561 on which epitaxial material is grown is NOT, as in applicants' claimed invention, subjected to "etching ... to remove same" (applicants' claim 70, line 4), but contrariwise **has the grown material removed therefrom, so that the base substrate can be reused** in subsequent growth processes.

Simply stated, applicants' claim 70 requires the base substrate **to be etched away from the deposited GaN material**, while Gmitter '561 **preserves the base substrate in original form**.

Gmitter '561 thus **teaches away from** applicants' invention. Such teaching away must be taken into consideration. See, for example, MPEP §2141.02, which requires that:

> **"[A] prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)."**

Based on such consideration of Gmitter '561 **as a whole**, Gmitter '561 fails to provide any derivative basis for applicants' invention as claimed in claim 70.

Claim 70 therefore is patentably distinguished over the disclosure of Gmitter '561.

Claim 71 is likewise patentable over Gmitter '561, as depending from claim 70.

In addition to such (dependency) basis of patentability, claim 71 is otherwise also patentable over Gmitter '561 by recital of a method

> **"wherein the gallium arsenide substrate is etched away *in situ* at a temperature within 300°C of the growth temperature of the GaN on the gallium arsenide substrate" (claim 71, lines 1-3)**

Gmitter `561 **lacks any teaching or suggestion of such methodology**. It is to be noted that the growth temperature of gallium nitride may be on the order of 800-1300°C, as disclosed at page 10, lines 8-9 of the instant specification. Thus, the etching away of the base substrate in accordance with applicants' claimed invention takes place at high elevated temperature, e.g., of 500-1000°C.

Gmitter '561, as discussed hereinabove, **fails to disclose etching away of the base substrate on which material is grown**, and in fact **teaches away** from such approach, by disclosure of a methodology that is carried out for the purpose of

> **"leaving the expensive single crystal original substrate available for re-use" (Gmitter '561, column 4, lines 61-62).**

Gmitter '561 lacks any teaching or suggestion of etching away the original substrate.

Additionally, the only etching that is taught in Gmitter '561 is the etching of the thin release layer[1] of Gmitter '561, which Gmitter '561 teaches to be carried out at "reduced temperatures, e.g., about 0°C" (Gmitter '561, column 6, line 33). This is a further teaching away, and underscores the lack of basis in Gmitter '561 for applicants' invention as claimed in claim 71.

Concerning the contention at page 8 of the September 15, 2003 Office Action that the temperature recited in claim 71 is an optimization obtainable by routine experimentation and an obvious selection of parameters, MPEP §2144.05 and In re Aller **are inapplicable to the proper consideration of claim 71**.

MPEP §2144.05 cites In re Aller for the proposition that

> **"[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955)" (MPEP §2144.05).**

[1] having a thickness of "less than 100 nm and ... as thin as 2 nm" (column 4, lines 58-59 of Gmitter '561).

Here, the general conditions of the applicants' claim (viz., temperature within 300°C of the growth temperature) are NOT disclosed in the prior art, since Gmitter '561 in fact **teaches away** from such high elevated temperature by disclosure of "reduced temperatures, e.g., about 0°C" (Gmitter '561, column 6, line 33), as the temperature for the etching operation, which etching operation, however, involves etching of a **release layer**, and NOT the etching of an **original substrate**.

For all these reasons, Gmitter `561 fails to teach or suggest applicants' claimed invention.

The Examiner therefore is respectfully requested to withdraw the rejection of claims 70-71.

Fees Payable for Terminal Disclaimer

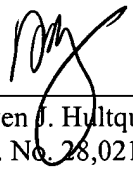
The Terminal Disclaimer fee of $110.00, for the Terminal Disclaimer submitted herewith, is authorized to be charged pursuant to the enclosed Credit Card Authorization Form.

Authorization also is hereby given to charge any additional fees or amounts necessary for the entry of this response, to Deposit Account Number 08-3284 of Intellectual Property/Technology Law.

CONCLUSION

Based on all of the foregoing, claims 61, 63-67 and 70-71 are now in form and condition for allowance. The Examiner is respectfully requested to reconsider and allow such claims. If any additional issues remain, incident to the formal allowance of the application, the examiner is requested to contact the undersigned attorney at (919) 419-9350 to discuss same, in order that this application may be passed to issue at an early date.

Respectfully submitted,



Steven J. Hultquist
Reg. No. 28,021
Attorney for Applicants

**INTELLECTUAL PROPERTY/
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Attorney File No.: 2771-161 CON 2**

OIPE JC110 DEC 15 2003 PATENT & TRADEMARK OFFICE

Patent Application
2771-161 CON2 (7483)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re United States Patent Application of:		**Docket No.:**	**2771-161 CON 2**
Applicant:	**TISCHLER, Michael A., et al.**	**Examiner:**	**SONG, Matthew J.**
Application No.:	**09/929,789**	**Art Group:**	**1765**
Date Filed:	**August 14, 2001**	**Confirm. No.:**	**1145**
Title:	**BULK SINGLE CRYSTAL GALLIUM NITRIDE AND METHOD OF MAKING SAME**		**25559**

EXPRESS MAIL CERTIFICATE

I hereby certify that I am mailing the attached documents to the Commissioner for Patents on the date specified, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, and Express Mailed under the provisions of 37 CFR 1.10.

L. Stephen Lockett
Name: L. Stephen Lockett

December 15, 2003
Date

EV 387840525 US
Express Mail Label Number

DECLARATION OF MICHAEL A. TISCHLER UNDER 37 CFR §1.131 FOR UNITED STATES PATENT APPLICATION NO. 09/929,789

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

MICHAEL A. TISCHLER, being duly cognizant of the provisions and requirements of 37 CFR 1.131, hereby declares:

1. THAT I am a named co-inventor of the subject matter disclosed and claimed in U.S. Patent Application No. 09/929,789, filed August 14, 2001 in the United States Patent and Trademark

Office in the names of Michael A. Tischler, Thomas F. Kuech and Robert P. Vaudo, for "Bulk Single Crystal Gallium Nitride and Method of Making Same" (the "Application"), which is a continuation of U.S. Patent Application No. 08/955,168 filed October 21, 1997, now abandoned (the "Parent Application"), which is a continuation-in-part of U.S. Patent Application No. 08/188,469 filed January 27, 1994, now U.S. Patent No. 5,679,152 (the "Grandparent Application"), and that such invention was made in the course and scope of my employment by ADVANCED TECHNOLOGY MATERIALS, INC. (hereafter "ATMI"), 7 Commerce Drive, Danbury, CT 06810, which is the owner by assignment of the invention, the Application, the Parent Application and the Grandparent Application.

2. THAT the Application discloses and claims a method of making a single crystal GaN substrate, comprising growing GaN over a substrate heterogeneous to GaN, and removing the heterogeneous substrate to yield the single crystal GaN substrate.

3. THAT I am aware that the various claims now pending in the application have been rejected in the September 15, 2003 Office Action under 35 USC 102(e) as anticipated by U.S. Patent 5,846,844, issued December 8, 1998 to Isamu Akasaki, Kazumasa Hiramatsu, and Theeradetch Detchprohm, claiming priority of U.S. Patent Application No. 08/158,252 filed November 29, 1993, now abandoned (hereafter "Akasaki").

4. THAT the invention of the Application was conceived prior to the effective date of Akasaki and was coupled with due diligence from prior to the effective date of Akasaki to the filing date of the Application.

5. THAT in support of the factual statement made in paragraph 4 above, attached hereto in Exhibit 1 hereof is a true and exact copy of Record of Invention No. [redacted], on which all dates have been blacked out, but which dates are prior to the Akasaki priority date.

6. THAT the ROI explains that prior to the present invention, no bulk GaN substrate "material exists or has been produced." Towards that end, the "general idea presented [in the ROI] . . . is to use a sacrificial substrate upon which is nucleated GaN . . . or associated compounds. The III-V nitride layer is grown on the substrate to the desired thickness and then the substrate is etched away, in situ, at temperatures close to the growth temperature," yielding a bulk GaN substrate material. Further, the ROI discloses the use of a "buffer layer" on the substrate "to provide a clean nucleation layer for subsequent growth."

7. THAT also included herewith is Exhibit 2, which is the cover page of a facsimile from ATMI's patent representative Janet Elliott to Steven J. Hultquist (hereafter "Attorney of Record") transmitted on November 12, 1993, which is immediately prior to the priority date of Akasaki. The body of the facsimile transmission included additional GaN substrate information provided by Thomas Kuech, a co-inventor of the Application.

8. THAT also included herewith is Exhibit 3, which is additional proprietary information ATMI faxed to Attorney of Record on January 18, 1994, to assist with the preparation of the Application.

9. THAT Application was filed on January 27, 1994.

10. THAT the ROI and facts attested to above evidence that the invention claimed in the Application was conceived prior to the priority date of Akasaki and was coupled with due diligence from prior to the priority date of Akasaki to the filing date of the Application.

11. THAT this Declaration is submitted as evidence antedating Akasaki to remove it as a reference against the claims of the Application.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine and imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent(s) issued thereon.

Michael A. Tischler

December 12, 2003
Date

EXHIBIT 1

INVENTION DISCLOSURE

ROI Number [redacted]

Short, Descriptive Title Method for producing bulk GaN substrates

(1) State the PROBLEM or DEFICIENCY which is overcome by your invention:
GaN, the related binary's AlN and InN and the associated ternary and quaternary compounds are of interest for blue and UV light emitters as well as electronic devices, especially those operating at high temperature or producing high power. The main advantages of the III-V nitrides are (1) they have a direct bandgap and (2) GaN and AlN form a closely lattice-matched ternary system similar to GaAs/AlAs. The main problem with using these materials is that there is no good, lattice-matched substrate. GaN would be ideal, but no such bulk material exists or has been produced. Thus heteroepitaxial growth on a different substrate is the approach used.

Two types of defects arise as a result of heteroepitaxial growth. The first is dislocations due to the lattice mismatch between the III-V nitride layer and the substrate. The typical substrate is sapphire, which has a 13.8% lattice mismatch to GaN. SiC is a closer lattice match =3%, but it is still quite large. Many other substrates have been used, but all of them have large lattice mismatches and result in a high density of defects in the grown layers. The second kind of defect is dislocations generated during cool-down after growth as a result of different thermal coefficients of expansion. In this disclosure, we describe a method for producing large area, single crystal GaN substrates.

(2) Describe clearly the INVENTION, RESULTS, ADVANTAGES. (Make DRAWINGS when possible and DESCRIBE FULLY the invention and its OPERATION using REFERENCE NUMERALS to indicate elements.
The general idea presented in this disclosure is to use a sacrificial substrate upon which is nucleated the GaN, AlN, InN or associated compounds. The III-V nitride layer is grown on the substrate to the desired thickness and then the substrate is etched away, in-situ, at temperatures close to the growth temperature. Dislocations arising from the lattice mismatch are reduced in

INVENTOR(S):

(Signature)	(Signature)	(Signature)
Michael A. Tischler		
(Print Name)	(Print Name)	(Print Name)
[redacted]		
(Date)	(Date)	(Date)

READ AND UNDERSTOOD BY:

(Signature - Full Name)	(Signature - Full Name)
Joan Ellis	
(Print or Type Full Name)	(Print or Type Full Name)
[redacted]	
(Date)	(Date)

density by growing thick layers. It is known that the misfit dislocation density decreases with epitaxial layer thickness, and in this case very thick (25-1000μm) layers will be grown. The misfit dislocation density can be further reduced by using previously grown III-V nitrides as a substrate. Dislocations due to the different thermal coefficients of expansion are eliminated by in-situ etching of the substrate at the growth temperature. The in-situ etching is done by the introduction of chlorinated or fluorinated species (i.e. HCl, HF, etc.) which will etch the sacrificial substrate much faster than the III-V nitride. Ideally, the growth of the III-V nitride layer would be done in a kinetically limited regime, which would permit stacking of the substrates in a furnace for simultaneous growth on a large number of substrates.

In a specific embodiment, the sacrificial substrate is silicon and the substrate to be produced is GaN. Growth begins by heating the silicon to the growth temperature (in the range of 800-1300°C) and introducing the growth precursors. In one preferred method, this would first consist of the growth of a silicon buffer layer on the silicon substrate to provide a clean nucleation layer for subsequent growth. The silicon precursors are then turned off and the GaN precursors turned on. An example of such precursors are trimethyl gallium and ammonia. The GaN layer is grown to the desired thickness (25-1000μm) and the GaN precursors are turned off. Then the etching species is introduced (in this case HCl) and the silicon substrate is removed. The etching time can be reduced by using pre-thinned sacrificial substrates. The remaining GaN layer is then cooled and removed from the reactor.

Other materials that can be grown this way include AlN, InN as well as ternary and quaternary alloys of these and GaN binary's. SiC could also be grown using this technique. Some suitable substrates include silicon, GaAs and InP.

It is possible that the constituents of the sacrificial substrate may act as a dopant for the desired substrate layer. If this is the case, the back side of the sacrificial substrate could be covered with a mask such as silicon dioxide or silicon nitride to prevent autodoping of the growth layer. However, there will be some diffusion of the sacrificial substrate material into the desired grown layer. This could be beneficial, for example in the case of a sacrificial silicon substrate and a grown GaN layer, the silicon would form a heavily doped n-type layer at the back of the

INVENTOR(S):

(Signature)	(Signature)	(Signature)
Michael A. Tischler		
(Print Name)	(Print Name)	(Print Name)
[redacted]		
(Date)	(Date)	(Date)

READ AND UNDERSTOOD BY:

(Signature - Full Name)	(Signature - Full Name)
Janet Elliott	
(Print or Type Full Name)	(Print or Type Full Name)
[redacted]	
(Date)	(Date)

substrate which would be advantageous for forming n-type ohmic contacts. If this layer were not desired, it could be etched or polished off after growth.

The advantages of this technique are:

1. Large diameter substrates can be produced. The limit is the available size of the sacrificial substrate. For example if the sacrificial substrate is silicon, this could produce substrates greater than 10" in diameter.

2. The substrates are essentially ready for subsequent processing after growth. No coring, orienting flatting etc. is required as in bulk growth. Some minor polishing may be required.

3. Many substrates can be produced simultaneously.

4. No defects from thermal coefficient of expansion differences are produced.

5. The defect density can be further removed by using a previously grown desired substrate (which is lattice matched) instead a homoepitaxial substrate.

6. Heavily doped back contact layers for ohmic contacts are easily produced.

7. Substrates of varying compositions can be easily produced. For example ternary substrates can be produced easily because the composition is controlled by the gas phased composition. This is much easier than composition control when growth occurs from a liquid melt. Substrates with compositional variations can also be easily produced.

7. The doping density in the substrates can be easily controlled, again by gas phase composition control. No problems associated with segregation coefficient issues are involved. In addition, the doping in the substrate can be varied, if desired, throughout the thickness of the substrate.

8. In a potential embodiment, the substrate and device structure could be grown in one cycle.

INVENTOR(S):

(Signature)	(Signature)	(Signature)
Michael A. Tischler		
(Print Name)	(Print Name)	(Print Name)
[redacted]		
(Date)	(Date)	(Date)

READ AND UNDERSTOOD BY:

(Signature - Full Name)		(Signature - Full Name)
Janet Elliott		
(Print or Type Full Name)		(Print or Type Full Name)
[redacted]		
(Date)		(Date)

(3) Was this invention fi.t conceived or first actually reduc.l to practice under government contract support? If so, what are the contract name and contract number? No

(4) Has there been any publication, public disclosure, or offer for sale, or are any contemplated? Provide details, especially dates.
This invention was made with Tom Kuech, and he has mentioned the idea to Kurt Gaskill of NRL.

(5) Laboratory Notebook or Runsheet Number cross reference, including date(s).
Book 289, pp. 49-60.

INVENTOR(S):

(Signature)	(Signature)	(Signature)
Michael A. Tischler		
(Print Name)	(Print Name)	(Print Name)
[redacted]		
(Date)	(Date)	(Date)

READ AND UNDERSTOOD BY:

(Signature - Full Name)	(Signature - Full Name)
Janet Elliott	
(Print or Type Full Name)	(Print or Type Full Name)
[redacted]	
(Date)	(Date)

EXHIBIT 2

Patent Application
2771-161 CON2 (7483)

FAX TRANSMISSION

Advanced Technology Materials

7 Commerce Drive ◆ Danbury, CT 06810-4169
Phone 203-794-1100 ◆ Fax 203-830-4119

TO: Steve

COMPANY:

FROM: John

DATE AND TIME OF TRANSMISSION:

MESSAGE:

Here's the letter from Tom Kuech on GaN substrate.
Do we have a file number?

FAX NO:

This transmission is 1 pages including cover page.

EXHIBIT 3

c. Identification and Significance of the Problem or Opportunity

The III-V nitrides, GaN, AlN and InN and their associated ternary and quaternary compounds, are of interest for blue and UV light emitters as well as electronic devices operating at high temperature or high power. The primary advantages of the III-V nitrides are a direct bandgaps ranging from 2.09 to 6.2EV and a closely lattice matched ternary system – GaN and AlN form a closely lattice-matched ternary system similar to GaAs/AlAs. The main problem with the nitrides is the lack of a lattice-matched substrate.

GaN would be the ideal substrate, but no bulk GaN material exists or has ever been produced. GaN is unstable at elevated temperature and has only limited solubility in Ga melts. Consequently, GaN has only been grown heteroepitaxially on foreign substrates.

Many substrates have been used for the deposition of GaN, including Si, GaAs and the most common, sapphire. Sapphire has a 13.8% lattice mismatch to GaN. SiC has a closer lattice match of ~3%; defect density in GaN epitaxial layers will be reduced but still may require buffer layers. Lattice mismatch between GaN and the substrate creates a dense network of defects at the interface which propagate into the grown layer. This yields poor morphology as well as a high density of structural and electrical defects.

Differences in the thermal coefficient of expansion (TCE) also create defects. This occurs during cooling of the epilayer-substrate system after growth, where the two films contract at different rates, causing stress and eventual defect formation. Again, these defects are electrically and optically active and result in poor quality material. Additionally, all of the stress may not be relieved by defect formation, resulting in wafer warpage and cracking, similar to the GaAs on Si system.

In this proposal, ATMI will examine a novel growth technique to produce low defect density GaN substrates. The key feature of this technique is the use of a sacrificial substrate which is removed from the deposited epitaxial GaN layer at the growth temperature. This will completely eliminate the formation of defects, wafer warpage or cracking resulting from differences in TCE. The misfit dislocation density will be reduced by growing thick layers of GaN (25-1000μm).

In addition to greatly reducing the defect density, this sacrificial substrate technique has other advantages. First, large diameter substrates can be produced; the diameter is limited only by the size of available sacrificial substrates. For a silicon sacrificial substrate, this technique could produce GaN substrates greater than 10" in diameter. Second, the substrates are essentially epi-ready, no substrate fabrication, i.e. sawing and polishing, is required as in traditional bulk growth. Third, substrates of varying compositions and doping density can be easily produced because these parameters are controlled by the gas phase deposition process. The doping can easily be varied throughout the thickness of the substrate, for example to produce a heavily doped layer at the back for low resistance ohmic contacts. The dopant could be introduced either from the